Memory Trends, Challenges and Solutions

Abstract:
Memory continues to be critical element in VLSI applications from big data to mobile to wearables and IoT. SRAM has been at the forefront of technology scaling for every process generation. As we move to sub 20nm technology, technologists and designers faces key challenges including bit cell area scaling, VDD/Vccmin scaling, leakage and dynamic power reduction, etc. In parallel, memory industry has been looking for emerging memory solutions to replace entrenched memory technologies including SRAM, DRAM and Flash. This talk will discuss the challenges and potential solutions for SRAM scaling and the memory trends in the emerging memory.

Biography:
Jonathan Chang is a director leading SRAM IP development at TSMC. He is responsible for delivering SRAM compilers, custom SRAM IPs for low power, high speed applications for advance technology nodes. Jonathan joined Intel Corporation, Santa Clara, CA in 1998 and since has been engaged in the design of several high-performance microprocessors with emphasis in large, high-speed, low power cache design. He was a Principal Engineer in the area of cache design in Enterprise Microprocessor Group. In 2010, Jonathan joined TSMC, Hsin-Chu, Taiwan.

Jonathan is a senior member of the IEEE and serves as a technical program committee member of Memory subcommittee for ISSCC since 2013. Jonathan also was the NAE (North America and Europe) technical program committee member of 2011 VLSI symposium on circuits and associate editor of IEEE Trans on VLSI. Jonathan has published 20+ technical papers in IEEE conferences or journals.

Jonathan Chang received the B.S. degree in electrical engineering from National Taiwan University, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA.